AMENDMENTS TO ABSTRACT

Please amend the Abstract of this invention beginning at page 49, line 2 as follows:

~~A freeway routing system for a field programmable gate array (FPGA) comprising a first FPGA tile. The first FPGA tile comprising a plurality of functional groups (FGs) arranged in rows and columns; a plurality of interface groups (IGs) surrounding the plurality of FGs such that one IG is positioned at each end of each row and column, each of the IGs having a first, second and third set of input ports and a first, second and third set of output ports. A freeway routine system including a set of routing conductors configured to transfer signals to said first, second and third input ports, and configured to transfer signals from said first, second and third output ports of The set of routing conductors comprising: a plurality of vertical conductors that form intersections with a plurality of horizontal conductors; and programmable interconnect elements located at said intersections in a diagonal orientation on said FPGA tile.~~

A freeway routing system that connects interface groups in said field programmable gate array. The freeway system having a first set of routing conductors configured to transfer signals to the input ports of at least one interface group in a first tile of the field programmable gate array and configured to transfer signals from the output ports of other tiles in the filed programmable gate array. The first set conductors include vertical conductors that form intersections horizontal conductors and programmable interconnect elements located at said intersections vertical conductors and horizontal conductors in a diagonal orientation to connect each of horizontal conductors to one of the vertical conductors.